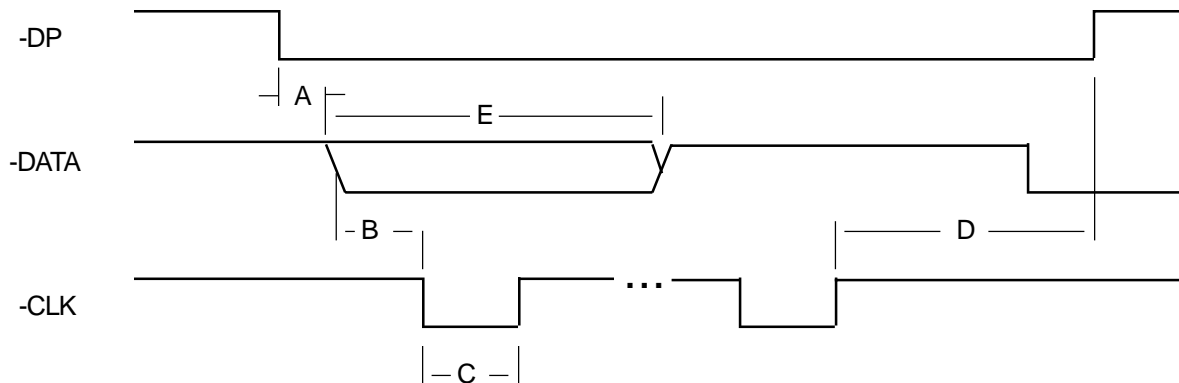
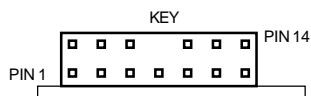


OUTPUT TIMING

- A 1us Min.
- B 1us
- C 12us
- D 18.4 to 36ms
- E Bit Cell Length

Pin Assignment**2x7 14 pin**

PIN	SIGNAL	
1	-DATA	Data bit Lo = Logic 1
2	(NC)	
3	-CLK	Clock LO data valid
4	(NC)	
5	-FCD	Front card detect
6	(NC)	
7	-RCD	Rear card detec
8	[KEY]	
9	+5V	
10	GND	
11	(NC)	
12	(NC)	
13	-DP	Data present
14	(NC)	